CONTENTS

SEMICONDUCTOR

ENERGY BANDS IN SOLIDS

Based on Pauli's exclusion principle

In an isolated atom electrons present in energy level but in solid, atoms are not isolated, there is interaction among each other, due to this energy level splited into different energy levels. Quantity of these different energy levels depends on the quantity of interacting atoms. Splitting of sharp and closely compact energy levels result into energy band. This is discrete in nature. Order of energy levels in a band is 10^{23} and their energy difference = 10^{-23} eV.

Energy Band

Range of energy possessed by electron in a solid is known as energy band.

Valence Band (VB)

Range of energies possessed by valence electron is known as valence band.

(a) Have bonded electron.

(b) No flow of current due to such electron.

(c) Always fulfill by electron.

Conduction Band (CB)

Range of energies possessed by free electron is known as conduction band.

(a) It has conducting electrons.

(b) Current flows due to such electrons.

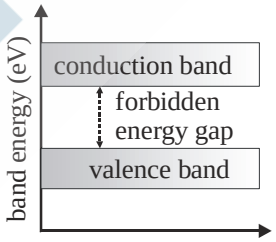
(c) If conduction band is fully empty then current conduction is not possible.

(d) Electrons may exist or not in it.

Forbidden Energy gap (FEG) (ΔE_g)

$$\Delta E_g = (C B)_{min} - (V B)_{max}$$

Energy gap between conduction band and valence band, where no free electron can exist.



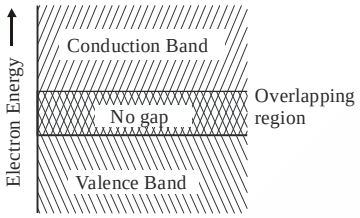
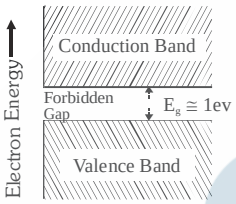
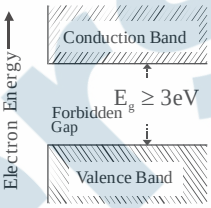
- Width of forbidden energy gap depends upon the nature of substance.
- Width is more, then valence electrons are strongly attached with nucleus
- Width of forbidden energy gap is represented in eV.
- As temperature increases forbidden energy gap decreases (very slightly).

CLASSIFICATION OF CONDUCTORS, INSULATORS AND SEMICONDUCTOR : -

On the basis of the relative values of electrical conductivity and energy bands the solids are broadly classified into three categories

(i) Conductor (ii) Semiconductor (iii) Insulator

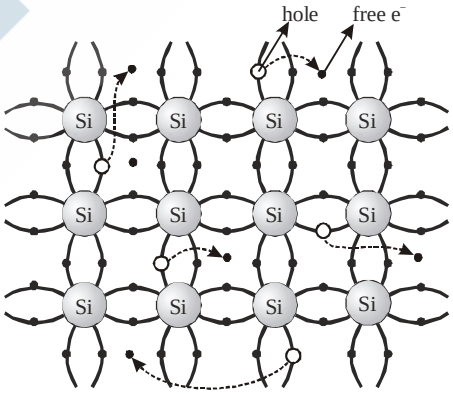
Comparison between conductor, semiconductor and insulator :

Properties	Conductor	Semiconductor	Insulator
Resistivity	$10^{-2} - 10^{-8}\ \Omega m$	$10^{-5} - 10^{6}\ \Omega m$	$10^{11} - 10^{19}\ \Omega m$
Conductivity	$10^{2} - 10^{8}$ mho/m	$10^{5} - 10^{-6}$ mho/m	$10^{-11} - 10^{-19}$ mho/m
Temp. Coefficient of resistance (α)	Positive	Negative	Negative
Current	Due to free electrons	Due to electrons and holes	No current
Energy band diagram	 Conductor	 Semi conductor	 Insulator
Forbidden energy gap	$\cong$ 0eV	$\cong$ 1eV	$\geq$ 3eV
Example :	Pt, Al, Cu, Ag	Ge, Si, GaAs, GaF_2	Wood, plastic, Diamond, Mica

CONCEPT OF "HOLES" IN SEMICONDUCTORS

Due to external energy (temp. or radiation) when electron goes from valence band to conduction band (i.e. bonded electrons becomes free) a vacancy of free e^- creats in valence band,

which has same charge as electron but positive. This positively charged vaccancy is termed as hole and shown in figure.



- It is deficiency of electron in VB.
- It acts as positive charge carrier.
- It's effective mass is more than electron.
- It's mobility is less than electron.

Note : Hole acts as virtual charge carrier, although it has no physical significance.

- Number of electrons reaching from VB to CB at temperature T kelvin

$$n = A\,T^{3/2}\ e^{-\frac{E_g}{2kT}} = AT^{3/2}\exp\left[-\frac{E_g}{2kT}\right]$$

where

k = Boltzmann constant = 1.38×10^{-23} J/K

T = absolute temperature

A = constant

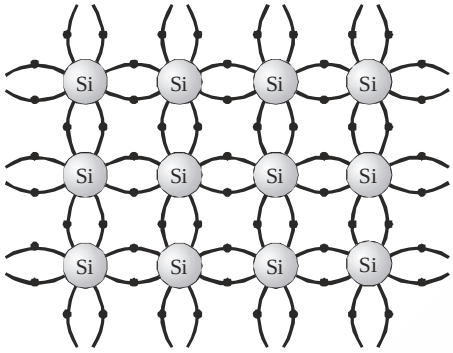
E_g = energy gap between CB and VB

- In silicon at room temperature out of 10^{12} Si atoms only one electron goes from VB to CB.
- In germanium at room temperature out of 10^{9} Ge atoms only one electron goes from VB to CB.

EFFECT OF TEMPERATURE ON SEMICONDUCTOR

At absolute zero kelvin temperature

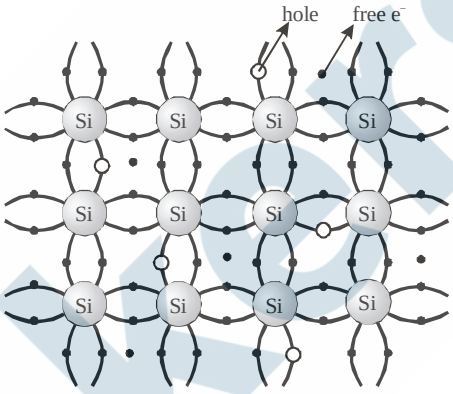
At this temperautre covalent bonds are very strong and there are no free electrons and semiconductor behaves as perfect insulator.



at 0 K
Valence band fully filled
Conduction band fully empty

Above absolute temperature

With increase in temperature few valence electrons jump into conduction band and hence it behaves as poor conductor.



at high temperature
Valence band partially empty
Conduction band partially filled

EFFECT OF IMPURITY IN SEMICONDUCTOR

Doping is a method of addition of "desirable" impurity atoms to pure semiconductor to increase conductivity of semiconductor. or

Doping is a process of deliberate addition of a desirable impurity atoms to a pure semiconductor to modify its properties in controlled manner.

Added impurity atoms are called dopants.

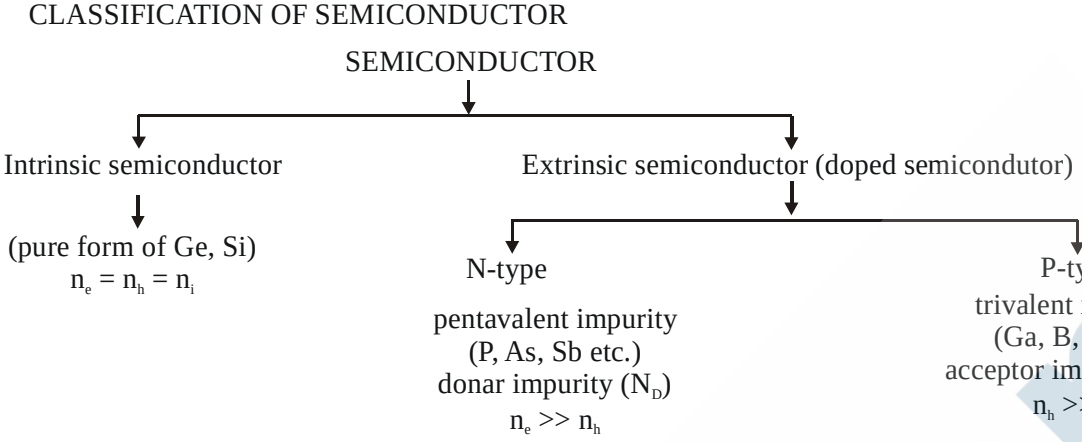
The impurity added may be ≈ 1 part per million (ppm).

- The dopant atom should take the position of semiconductor atom in the lattice.
- The presence of the dopant atom should not distort the crystal lattice.
- The size of the dopant atom should be almost the same as that of the crystal atom.
- The concentration of dopant atoms should not be large (not more than 1% of the crystal atom).

It is to be noted that the doping of a semiconductor increases its electrical conductivity to a great extent.

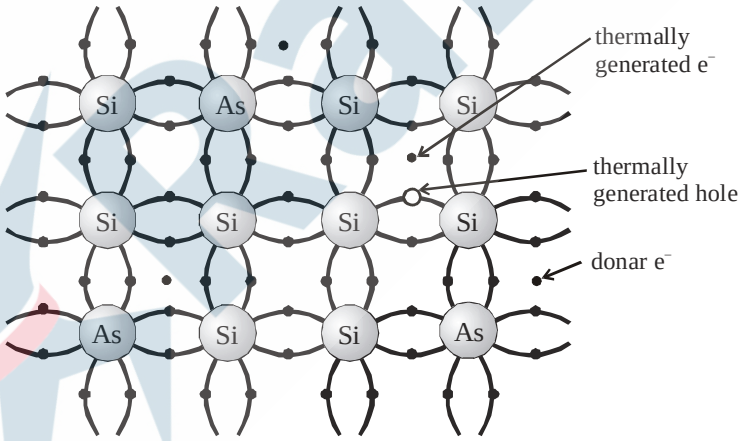
- The concentration of dopant atoms be very low, doping ratio is vary from impure : pure :: $1 : 10^6$ to $1 : 10^{10}$ In general it is $1 : 10^8$
- There are two main method of doping.
  (i) Alloy method (ii) Diffusion method (The best)
- The size of dopant atom (impurity) should be almost the same as that of crystal atom. So that crystalline structure of solid remain unchanged.

CLASSIFICATION OF SEMICONDUCTOR



N type semiconductor

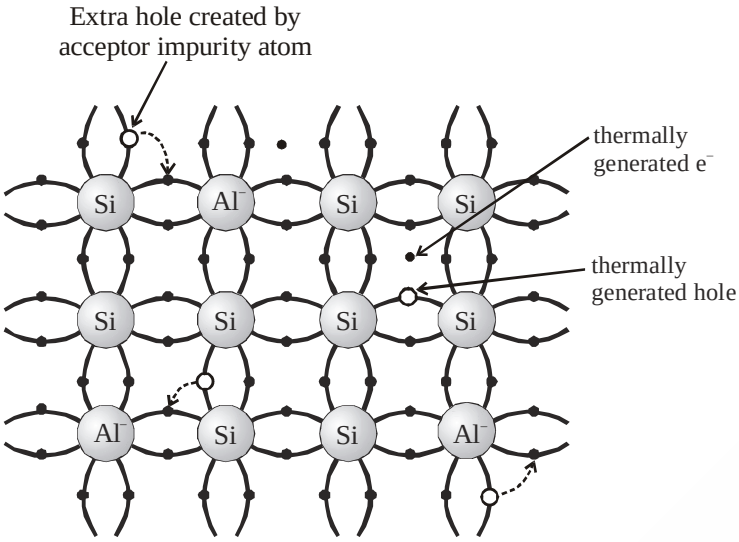
When a pure semiconductor (Si or Ge) is doped by pentavalent impurity (P, As, Sb, Bi) then four electrons out of the five valence electrons of impurity take part, in covalent bonding, with four silicon atoms surrounding it and the fifth electron is set free. These impurity atoms which donate free e^- for conduction are called as Donar impurity (N_D). Due to donar impurity free e^- increases very much so it is called as "N" type semiconductor. By donating e^- impurity atoms get positive charge and hence known as "Immobile Donar positive Ion". In N-type semiconductor free e^- are called as "majority" charge carriers and "holes" are called as "minority" charge carriers.



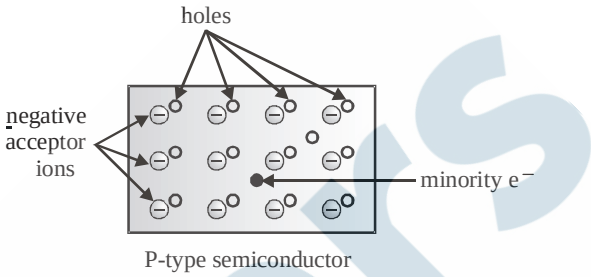
N-type semiconducting crystal

P type semiconductor

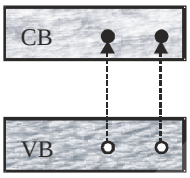
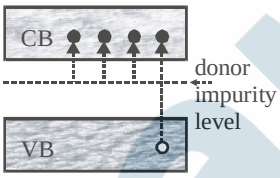
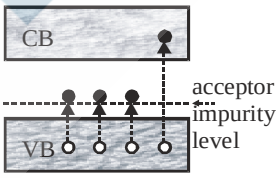
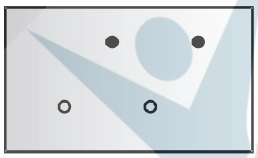
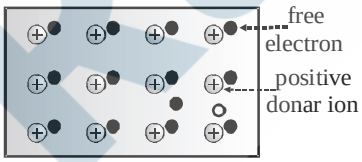
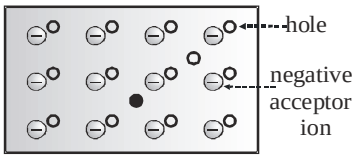
When a pure semiconductor (Si or Ge) is doped by trivalent impurity (B, Al, In, Ga) then outer most three electrons of the valence band of impurity take part, in covalent bonding with four silicon atoms surrounding it and except one electron from semiconductor and make hole in semiconductor. These impurity atoms which accept bonded e^- from valance band are called as Acceptor impurity (N_A). Here holes increases very much so it is called as "P" type semiconductor and impurity ions known as "Immobile Acceptor negative Ion". In P-type semiconductor free e^- are called as minority charge carries and holes are called as majority charge carriers.



P-type semiconducting crystal



P-type semiconductor

	Intrinsic Semiconductor	**N-type (Pentavalent impurity)**	**P-type(Trivalent impurity)**
1.			
2.			
3.	Current due to electron and hole	Mainly due to electrons	Mainly due to holes
4.	$n_e = n_h = n_i$	$n_h << n_e$ ($N_D \simeq n_e$)	$n_h >> n_e$ ($N_A \simeq n_h$)
5.	$I = I_e + I_h$	$I \simeq I_e$	$I \simeq I_h$
6.	Entirely neutral	Entirely neutral	Entirely neutral
7.	Quantity of electrons and holes are equal	Majority - Electrons Minority - Holes	Majority - Holes Minority - Electrons

Mass action Law

In semiconductors due to thermal effect, generation of free e⁻ and hole takes place.

Apart from the process of generation, recombination also occurs simultaneously, in which free e⁻ further recombine with hole.

At equilibrium rate of generation of charge carries is equal to rate of recombination of charge carrier.

The recombination occurs due to e^- colliding with a hole, larger value of n_e or n_h, higher is the probability of their recombination.

Hence for a given semiconductor rate of recombination $\propto n_e \times n_h$

so rate of recombination = $R\, n_e \times n_h$ R = recombination coefficient,

The value of R remains constant for a solid, according to the law of thermodynamics until crystalline lattice structure remains same.

For intrinsic semiconductor $n_e = n_h = n_i$

so rate of recombination = $R\, n_i^2$

$$R\, n_e \times n_h = R\, n_i^2 \quad \Rightarrow \quad n_i^2 = n_e \times n_h$$

Under thermal equilibrium, the product of the concentration 'n_e' of free electrons and the concentration n_h of holes is a constant and it is independent of the amount of doping by acceptor and donor impurities.

Thus from mass action law $\boxed{n_e \times n_h = n_1^2}$

Electron-hole Recombination :

It is necessarily to complete a band that electron is shared from neighbouring atoms or it may also be received from conduction band. In the second case electron recombines with the hole of valnce band. This process is known as electron-hole recombination.

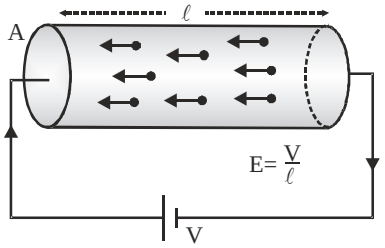
The breaking of bands or generation of electron-hole pairs, and completion of bands due to recombination is taking place continuously.

At equilibrium, the rate of generation becomes equal to the rate of recombination, giving a fixed number of free electrons and holes.

RESISTIVITY AND CONDUCTIVITY OF SEMICONDUCTOR

Conduction in conductor

Relation between current (I) and drift velocity (v_d)



$I = neAv_d$ n = number of electron in unit volume

A= cross sectional area

current density $J = \frac{I}{A}$ amp/m^2 = ne v_d drift velocity of electron $v_d = \mu E$

$J = ne\,\mu E$ $J = \sigma E$

Conductivity $\sigma = ne\mu = 1/\rho$ ρ = Resistivity

Mobility $\mu = \frac{v_d}{E}$

Conduction in Semiconductor

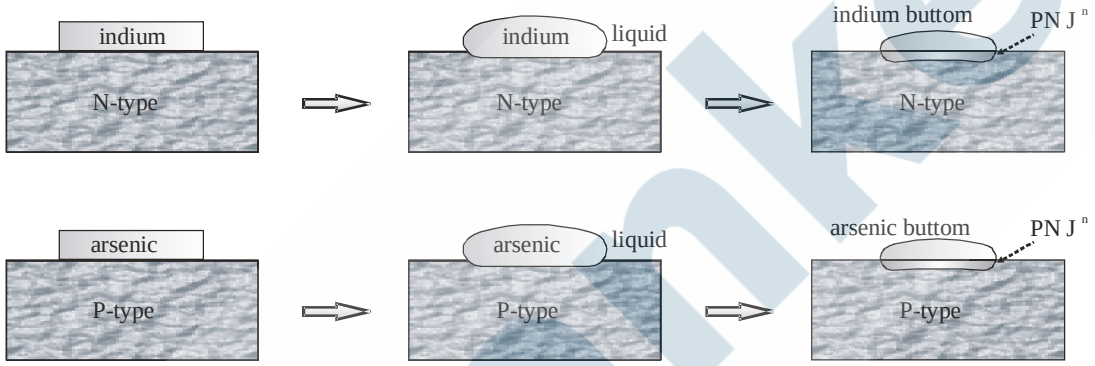
Intrinsic semiconductor	**P - type**	**N - type**
$n_e = n_h$	$n_h >> n_e$	$n_e >> n_h$
$J = ne [v_e + v_h]$	$J \cong e n_h v_h$	$J \cong e n_e v_e$
$\sigma = \frac{1}{\rho} = en [\mu_e + \mu_h]$	$\sigma = \frac{1}{\rho} \cong e n_h \mu_h$	$\sigma = \frac{1}{\rho} \cong e n_e \mu_e$

P - N JUNCTION

Techniques for making P-N junction

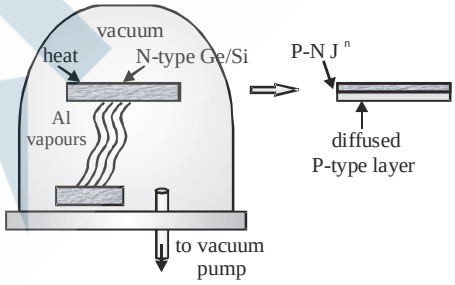
(i) Alloy Method or Alloy Junction

Here a small piece of III group impurity like indium is placed over n–Ge or n–Si and melted as shown in figure ultimetely P – N junction form.



(ii) Diffusion Junction :-

A heated P–type semiconductor is kept in pentavalent impurity vapours which diffuse into P–type semiconductor as shown and make P–N junction.



(iii) Vapour deposited junction or epitaxial junction :

If we want to grow a layer of n–Si or p–Si then p–Si wafer is kept in an atmosphere of Silane (a silicon compound which dissociates into Si at high temperatures) plus phosphorous vapours. On craking of silane at high temperature a fresh layer on n–Si grows on p–Si giving the "P–N junction". Since this junction growth is layer by so it is also referred as layer growth or epitaxial junction formation of P–N junction.

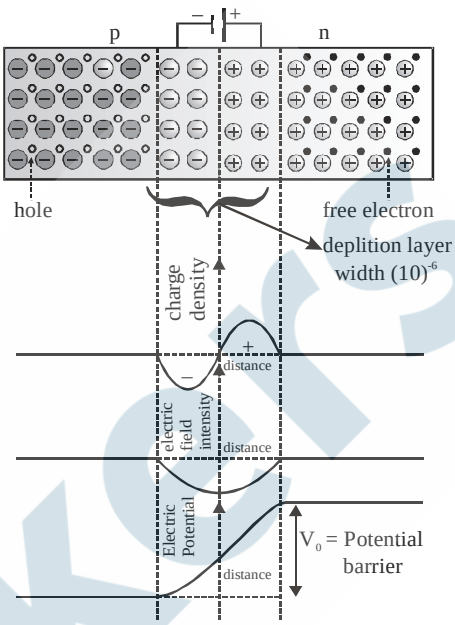
Description of P-N Junction without applied voltage or bias

Given diagram shows a P–N junction immediately after it is formed.

P region has mobile majority holes and immobile negatively charged impurity ions.

N region has mobile majority free electrons and immobile positively charged impurity ions.

Due to concentration difference diffusion of holes starts from P to N side and diffusion of e^- s starts N to P side.



Due to this a layer of only positive (in N side) and negative (in P–side) started to form which generate an electric field (N to P side) which oppose diffusion process, during diffusion magnitude of electric field increases due to this diffusion it gradually decreased and ultimately stope.

The layer of immobile positive and negative ions, which have no free electrons and holes called as **depletion layer** as shown in diagram.

- **Width of depletion layer $\cong 10^{-6}$ m**

  (a) As doping increases depletion layer decreases

  (b) As temperature is increased depletion layer also increases.

  (c) P-N junction $\rightarrow$ nonohmic, due to nonlinear relation between I and V.

- **Potential Barrier or contact potential**

  Ge $\longrightarrow$ 0.3 V Si $\longrightarrow$ 0.7 V

- Electric field, produce due to potential barrier $E = \frac{V}{d} = \frac{0.5}{10^{-6}} \Rightarrow E \cong 10^5$ V/m

  This field prevents the respective majority carrier from crossing barrier region

DIFFUSION AND DRIFT CURRENT

(1) Diffusion current – P to N side (2) Drift current – N to P side

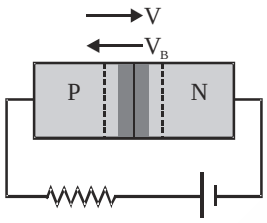
If there is no biasing diffusion current = drift current

So total current is zero

BEHAVIOUR OF P–N JUNCTION WITH AN EXTERNAL VOLTAGE APPLIED OR BIAS

Forward Bias

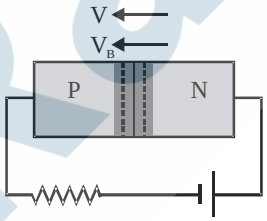
If we apply a voltage "V" such that P–side is positive and N–side is negative as shown in diagram.



The applied voltage is opposite to the junction barrier potential.Due to this effective potential barrier decreases, junction width also decreases, so more majority carriers will be allowed to flow across junction. It means the current flow in principally due to majority charge carriers and it is in the order of mA called as forward Bias.

Reverse Bias

If we apply a voltage "V" such that P–side is negative and N–side is positive as shown in diagram. The applied voltage is in same direction as the junction barrier potential. Due to this effective potential barrier increase junction, width also increases, so no majority carriers will be allowed to flow across junction.

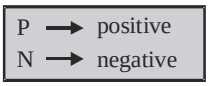
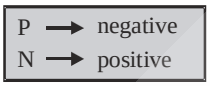
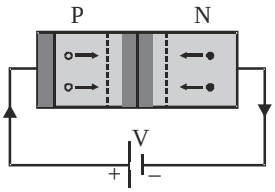
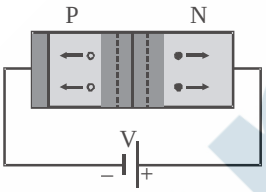
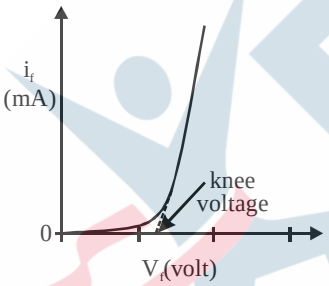
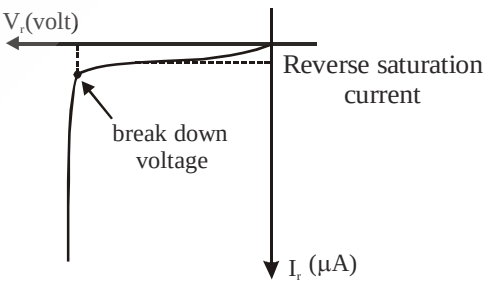


Only minority carriers will drifted. It means the current flow in principally due to minority charge carriers and is very small (in the order of μA). This bias is called as reversed Bias.

- In reverse bias, the current is very small and nearly constant with bias (termed as reverse saturation current). However interesting behaviour results in some special cases if the reverse bias is increased further beyond a certain limit, above particular high voltage breakdown of depletion layer started.
- Breakdown of a diode is of following two types :

  (i) Zener breakdown (ii) Avalanche breakdown

Comparison between Forward Bias and Reverse Bias

Forward Bias	Reverse Bias
	
	
1. Potential Barrier reduces	1. Potential Barrier increases.
2. Width of depletion layer decreases	2. Width of depletion layer increases.
3. P-N jn. provide very small resistance	3. P-N jn. provide high resistance
4 Forward current flows in the circuit	4. Very small current flows.
5. Order of forward current is milli ampere.	5. Order of current is micro ampere for Ge or Neno ampere for Si.
6. Current flows mainly due to majority carriers.	6. Current flows mainly due to minority carriers.
7. Forward characteristic curves.	7. Reverse characteristic curve
	
8. Forward resistance $R_f = \frac{\Delta V_f}{\Delta I_f} \cong 100\Omega$	8. Reverse resistance $R_r = \frac{\Delta V_r}{\Delta I_r} \cong 10^6\Omega$
9. Order of knee or cut in voltage Ge → 0.3 V Si → 0.7 V	9. Breakdown voltage Ge → 25 V Si → 35 V
Special point : Generally $\frac{R_r}{R_f} = 10^3 : 1$ for Ge	$\frac{R_r}{R_f} = 10^4 : 1$ for Si

Light Emitting Diode (LED):

A light emitting diode is simply a forward biased p-n junction which emits spontaneous light radiation. When forward bias is applied, the electron and holes at the junction recombine and energy released is emitted in the form of light. for visible radiation phosphorus doped GaAs is commonly used. The advantages of LEDs are:

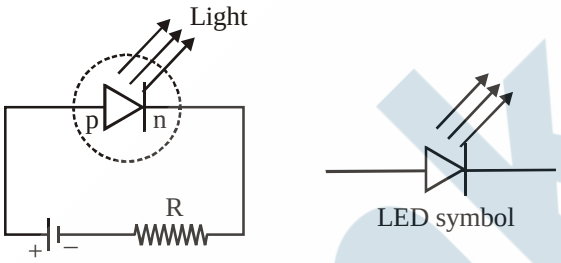
(i) Low operational voltage and less power.

(ii) Fast action with no warm up time.

(iii) Emitted light is nearly monochromatic.

(iv) They have long life.

I-V characterisitics of LED are similar to that of Si junction diode but the threshold voltages are much higher and slightly different for each colour. The reverse breakdown voltages of LED's are very low, about 5 V.

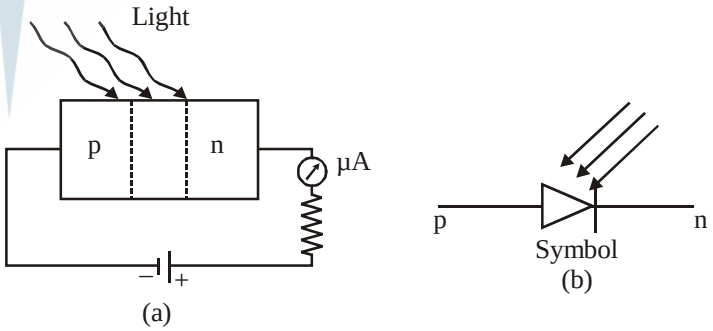


Photodiode:

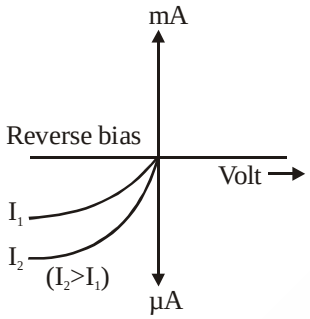
It is a reversed-biased p-n junction, illuminated by radiation. When p-n junction is reversed biased with no current, a very small reverse saturated current flows across the junction called the dark current. When the junction is illuminated with light, electron-hole pairs are created at the junction, due to which additional current begins to flow across the junction; the current is solely due to minority charge carriers.

(1) A photodiode is used in reverse bias, although in forward bias current is more than current in reverse bias because in reverse bias it is easier to observe change in current with change in light intensity.

(2) Photodiode is used to measure light intensity because reverse current increases with increase of intensity of light.

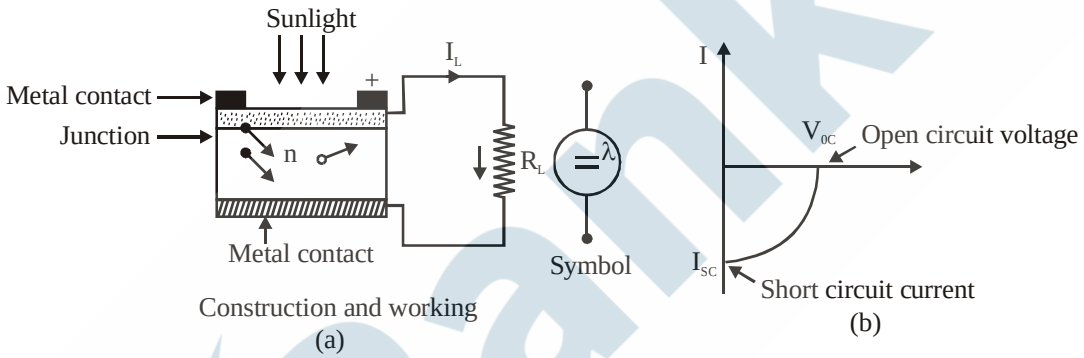


The characteristic curves of a photodiode for two different illurninatios I_1 and I_2 ($I_2 > I_1$) are shown in figure.



Solar Cell

A solar cell is a junction diode which converts tight energy' into electrical energy. A p-n junction solar cell consists of a large junction with no external biasing.



The surface layer of p-region is made very thin so that the incident photons may easily penetrate to reach the junction which is the active region. In an operation in the photovoltaic mode (i.e., generation of voltage due to bombardment of optical photons); the materials suitable for photocells are silicon (Si), gallium arsenide (GaAs), cadmium sulphide (CdS) and cadmium selenide (CdSe).

Working:

When photons of energy greater than band gap energy ($hv > E_g$) are made incident on the junction, electron-hole pairs are created which move in opposite directions due to junction field. These are collected at two sides of junction, thus producing photo-voltage; this gives rise to photocurrent. The characteristic curve of solar cell is shown in fig. Solar cells are used in satellites to recharge their batteries.

11. REVERSE BREAKDOWN

If the reverse bias voltage is made too high, the current through the PN junction increases rapidly at Y_z. The voltage at which this happens is called **breakdown voltage** or **Zener voltage.**

There two mechanism which causes this breakdown. One is called avalanche breakdown and other is called **Zener breakdown.**

Zener breakdown: When reverse bias is increased the electric field at then junction also increases. At some stage the electric field becomes so high that it breaks the covalent bonds creating electron, hole pairs, thus a large number of carriers are generated. This causes a large current to flow. This machanism is know as Zener breakdown.

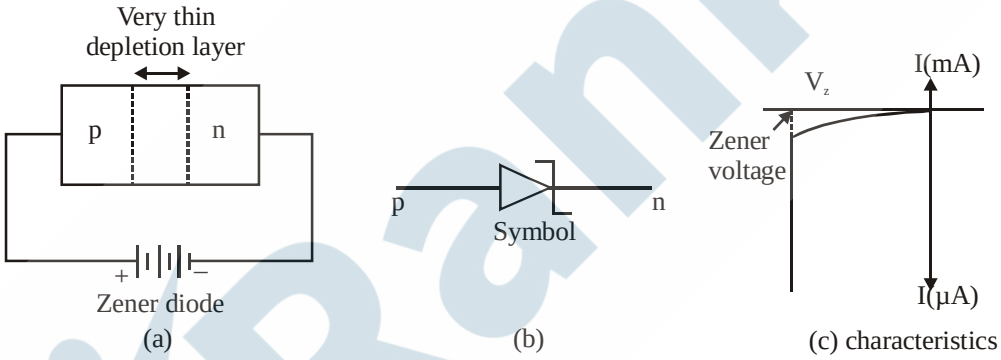
Avalanche breakdown : At high reverse voltage, due to high electric field, the rniniority charge carriers, while crossing the junction acquires very high velocities. These by collision breaks down the covalent bonds, generating more carriers. A chain reaction is established, giving rise to high current. This mechanism is called **avalanche breakdown..**

Zener Diode:

A zener diode is a specially designed heavily doped p-n junction, having a very thin depletion layer and having a very sharp breakdown voltage. It is always operated in breakdown region. Its breakdown voltage V_z is less than 6 V.

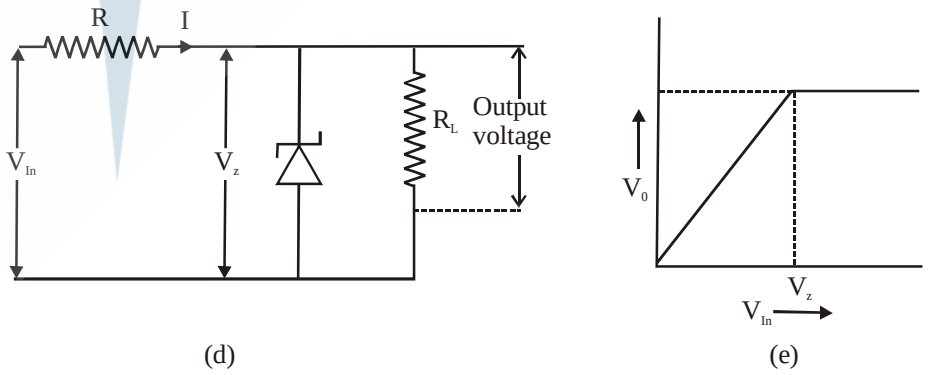
Zener Diode as a Voltage Regulator:

Zener diode may be used as a voltage regulator. The circuit of zener-diode is shown in figure.



In breakdown region the equation: $V_0 = V_z = V_{in} - RI$

Clearly, when the input voltage exceeds zener voltage to keep the voltage regularity, the extra input voltage appears across series resistance R. The voltage regulation curve is shown in figure.



Zener Break down

Where covalent bonds of depletion layer, its self break, due to high electric field of very high Reverse bias voltage.

very-very high reverse bias voltage.

This phenomena predominant

(i) At lower voltage after "break down"

(ii) In P – N having "High doping"

(iii) P – N Jn. having thin depletion layer

Here P – N not damage paramanently

"In D.C voltage stablizer zener phenomenan is used".

Avalanche Break down

Here covalent bonds of depletion layers are bro ken by collision of "Minorities" which aquire high kinetic energy from high electric field of

This phenomena predominant

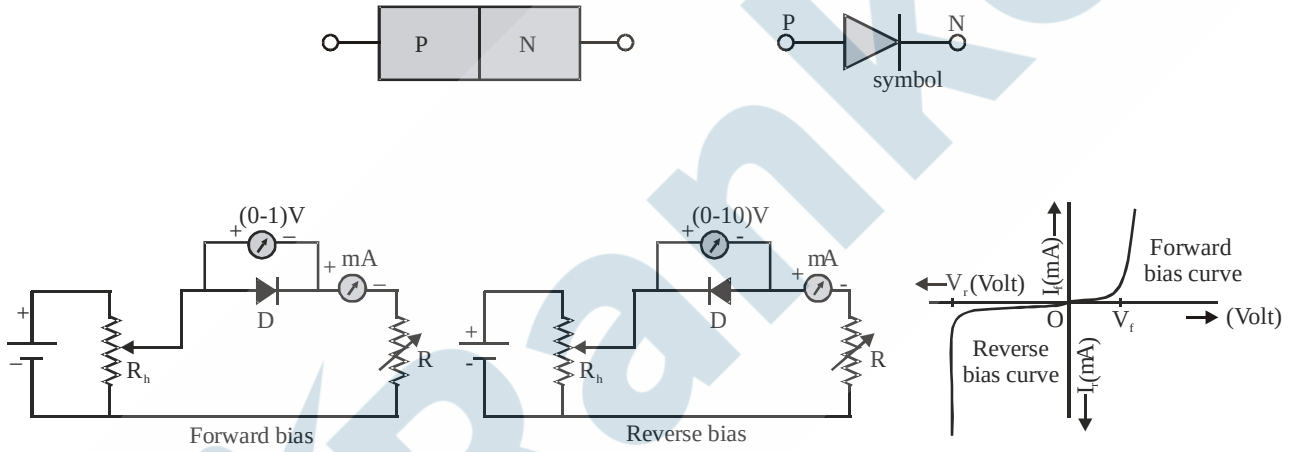
(i) At high voltage after breakdown

(ii) In P – N having "Low doping"

(iii) P – N Jn. having thick depletion layer

Here P – N damage peramanentaly due to "Heating effect" due to abruptly increment of minorities during repeatative collisoins.

CHARACTERISTIC CURVE OF P-N JUNCTION DIODE



In forward bias when voltage is increased from 0V is steps and corresponding value of current is measured, the curve comes as OB of figure. We may note that current increase very sharply after a certain voltage knee voltage. At this voltage, barrier potential is completely eliminated and diode offers a low resistance.

In reverse bias a microammeter has been used as current is very very small. When reverse voltage is increased from 0V and corresponding values of current measured the plot comes as OCD. We may note that reverse current is almost constant hence called reverse saturation current. It implies that diode resistance is very high. As reverse voltage reaches value V_B, called breakdown voltage, current increases very sharply.

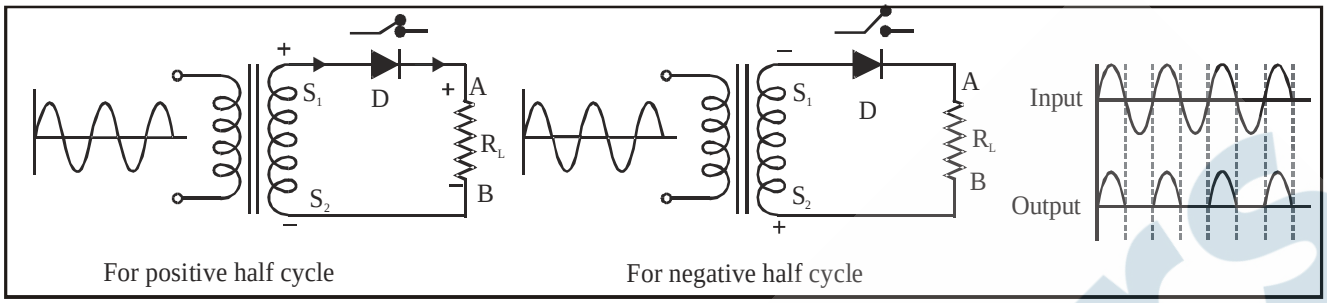
For Ideal Diode

in forward bias	in reverse bias
$R_f = 0$	$R_r = \infty$
'ON' switch	'OFF' switch

RECTIFIER

It is device which is used for converting alternating current into direct current.

Half wave rectifier



During the first half (positive) of the input signal, let S_1 is at positive and S_2 is at negative potential. So, the PN junction diode D is forward biased. The current flows through the load resistance R_L and output voltage is obtained.

During the second half (negative) of the input signal, S_1 and S_2 would be negative and positive respectively. The PN junction diode will be reversed biased. In this case, practically no current would flow through the load resistance. So, there will be no output voltage.

Thus, corresponding to an alternating input signal, we get a unidirectional pulsating output as shown.

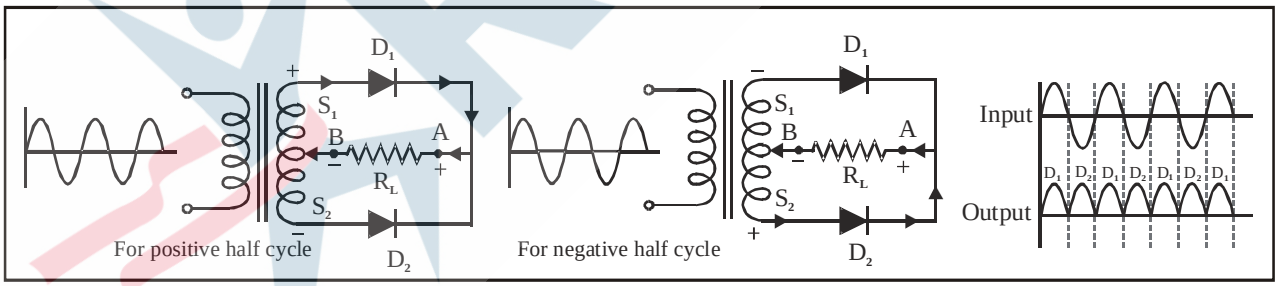
Peak inverse voltage (PIV)

In half wave rectifier PIV = maximum voltage across secondary coil of transformer (V_s)

= Peak value of output (V_m)

Full wave rectifier

When the diode rectifies the whole of the AC wave, it is called full wave rectifier. Figure shows the experiemental arrangement for using diode as full wave rectifier. The alternating signal is fed to the primary a transformer. The output signal appears across the load resistance R_L.



During the positive half of the input signal :

Let S_1 positive and S_2 negative.

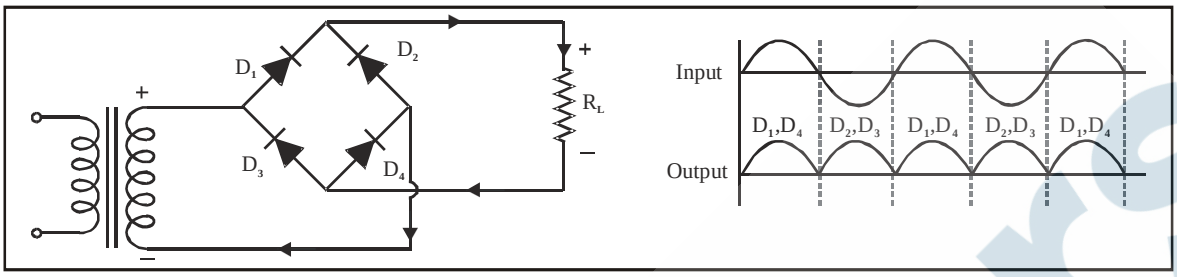
In this case diode D_1 is forward biased and D_2 is reverse biased. So only D_1 conducts and hence the flow of current in the load resistance R_L is from A to B.

During the negative half of the input signal :

Now S_1 is negative and S_2 is positive. So D_1 is reverse-biased and D_2 is forward biased. So only D_2 conducts and hence the current flows through the load resistance R_L from A to B.

It is clear that whether the input signal is positive or negative, the current always flows through the load resistance in the same direction and full wave rectification is obtained.

Bridge Rectifier



TRANSISTOR

Inventor William Bradford Shockley, John Bardeen and Walter Houser Brattain.

Transistor is a three terminal device which transfers a signal from low resistance circuit to high resistance circuit.

It is formed when a thin layer of one type of extrinsic semiconductor (P or N type) is sandwitched between two thick layers of other type of extrinsic semiconductor.

Each transistor have three terminals which are :-

(i) Emitter

(ii) Base

(iii) Collector

Emitter

It is the left most part of the transistor. It emits the majority carrier towards base. It is highly doped and medium in size.

Base

It is the middle part of transistor which is sandwitched by emitter (E) and collector (C). It is lightly doped and very thin in size.

Collector

It is right part of the transistor which collect the majority carriers emitted by emitter. It has large size and moderate doping.

There are two semiconducting PN-junctions in a transistor

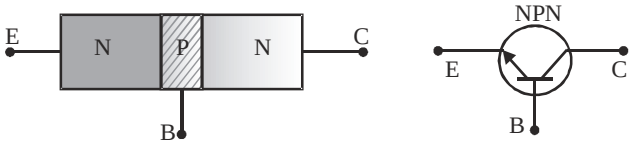
(i) The junction between emitter and base is known as emitter-base junction **(J_{EB})**.

(ii) The junction between base and collecter is known as base-collector junction **(J_{CB})**.

TRANSISTOR ARE OF TWO TYPES

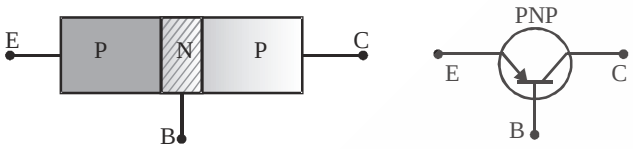
N-P-N Transistor

If a thin layer of P-type semiconductor is sandwitched between two thick layers of N-type semiconductor is known as NPN transistor.

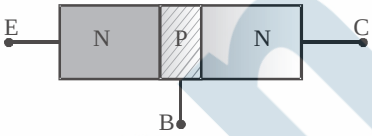


P-N-P Transistor

If a thin layer of N-type of semiconductor is sandwitched between two thick layer of P-type semiconductor is known as PNP transistor.



- Transistor have two P-N Junction J_{EB} and J_{CB}, therefore it can be biased in four following ways as given below:



Emitter-Base	Collector-Base	Region of working
Forward biased	Reverse biased	Active
Reverse biased	Forward biased	Inverse Active
Reverse biased	Reverse biased	Cut off
Forward biased	Forward biased	Saturation

- Comparsion between E, B and C

Emitter	Medium size	High dopping
Base	Smallest size	Low dopping
Collector	Largest size	Medium dopping

- The collector region is made physically larger than the emitter. Because collector has to dissipiate much greater power.

- Transistor all mostly work in active region in electronic devices & transistor work as an amplifier in Active region only.

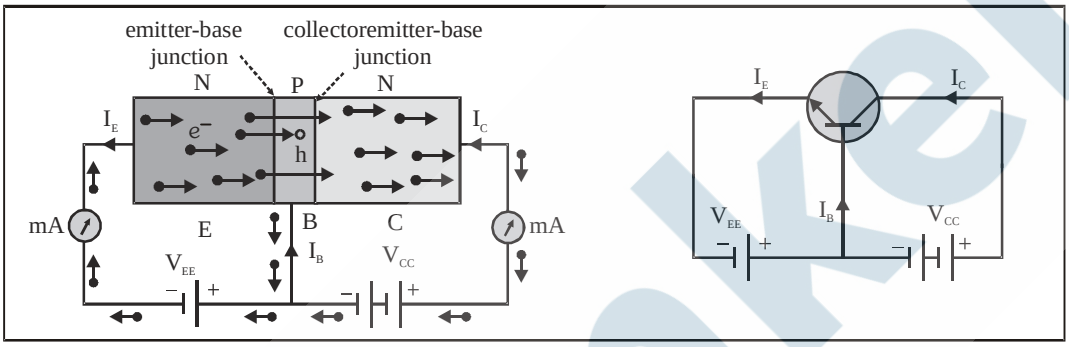
- Transistor i.e. It is a short form of two words "Transfer resistors". Signal is introduced at low resistance circuit and out put is taken at high resistance circuit.

- Base is lightly doped. Otherwise the most of the charge carrier from the emitter recombine in base region and not reaches at collector.

- Transistor is a current operated device i.e. the action of transistor is controlled by the motion of charge carriers. i.e. current.

WORKING OF NPN TRANSISTOR

The emitter Base junction is forward bias and collector base junction is reversed biased of n-p-n transistor in circuit (A) and symbolic representation is shown in Figure.



When emitter base junction is forward bias, electrons (majority carriers) in emitter are repelled toward base.

The barrier of emitter base junction is reduced and the electron enter the base, about 5% of these electron recombine with hole in base region result in small current (I_b).

The remaining electron ($\approx 95\%$) enter the collector region because they are attracted towards the positive terminal of battery.

For each electron entering the positive terminal of the battery is connected with collector base junction an electron from negative terminal of the battery connected with emitter base junction enters the region.

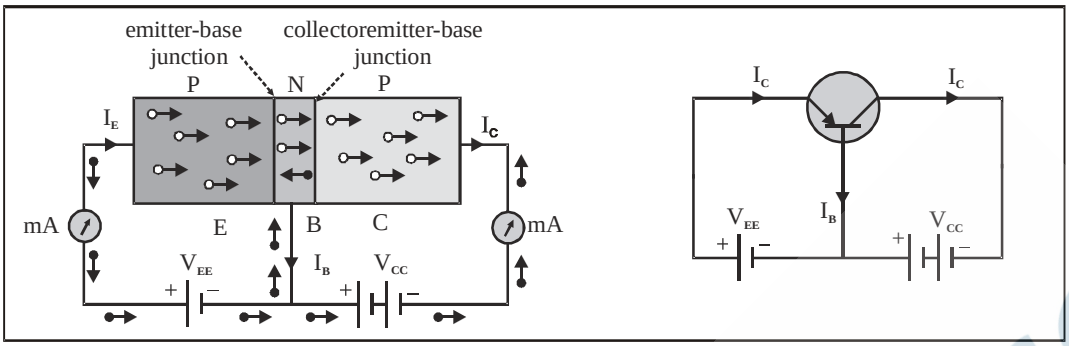
The emitter current (I_e) is more than the collector (I_c).

The base current is the difference between I_e and I_c and proportional to the number of electron hole recombination in the base.

$$I_e = I_b + I_c$$

WORKING OF PNP TRANSISTOR

When emitter-base junction is forward biased holes (majority carriers) in the emitter are repelled towards the base and diffuse through the emitter base junction. The barrier potential of emitter-base junction decreases and hole enter the n-region (i.e. base). A small number of holes ($\approx 5\%$) combine with electron of base-region resulting small current (I_b). The remaining hole ($\approx 95\%$) enter into the collector region because they are attracted towards negative terminal of the battery connected with the collector-base junction. These hole constitute the collector current (I_c).



As one hole reaches the collector, it is neutralized by the battery. As soon as one electron and a hole is neutralized in collector a covalent bond is broken in emitter region. The electron hole pair is produced. The released electron enter the positive terminal of battery and hole more towards the collector.

Basic Transistor Circuit Configurations :-

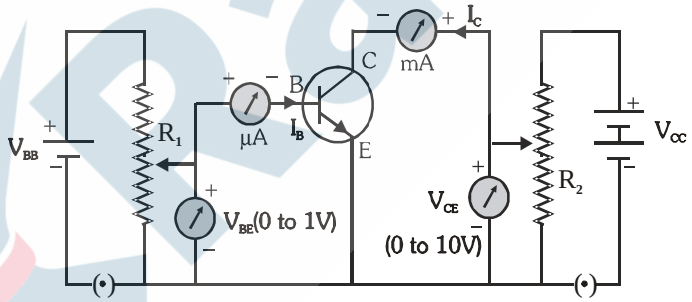
To study about the characterstics of transistor we have to make a circuit [In which four terminals are required]. But the transistor have three terminals, so one of the terminal of transistor is made common in input and output both. Thus, we have three possible configuration of transistor circuit.

(i) Common base (ii) Common emitter (iii) Common collector

In these three common emitter is widely used and common collector is rarely used.

Common emitter characterstics of a transistor

Circuit Diagram :



Circuit diagram for characteristic curve of n-p-n transistor in CE mode

Input characterstics

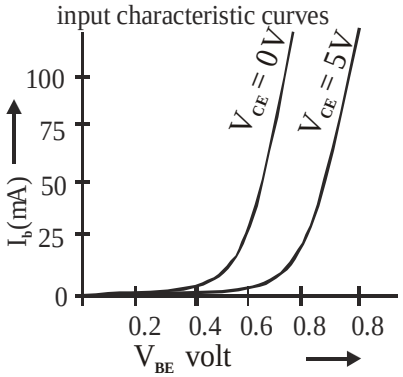
The variation of base current (I_b) (input) with base emitter voltage (V_{EB}) at constant-emitter voltage (V_{CE}) is called input characterstic.

(i) Keep the collector-emitter voltage (V_{CE}) constant (say V_{CE} = 1V)

(ii) Now change emitter base voltage by R_1 and note the corresponding value of base current (I_b).

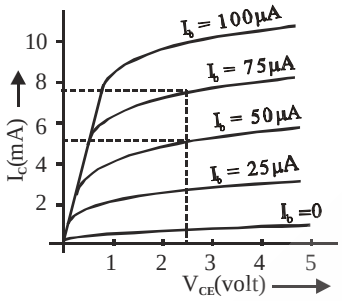
(iii) Plot the graph between V_{EB} and I_b.

(iv) A set of such curves can be plotted at different (V_{CE} = 2V)



Output characterstics

The variation of collector current I_c (output) with collector-emitter voltage (V_{CE}) at constant base current (I_b) is called output characterstic.



(i) Keep the base current (I_b) constant (say $I_b = 10\mu A$)

(ii) Now change the collector-emitter voltage (V_{CE}) using variable resistance R_2 and note the corresponding values of collector current (I_c).

(iii) Plot the graph between (V_{CE} versus I_c)

(iv) A set of such curves can be plotted at different fixed values of base current (say 0, 20 μA, 30 μA etc.)

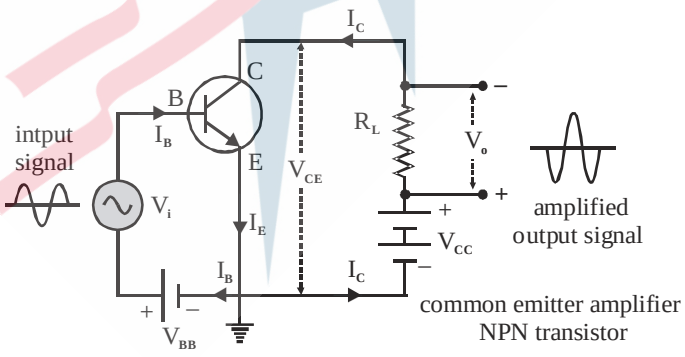
TRANSISTOR AS AN AMPLIFIER

The process of increasing the amplitude of input signal without distorting its wave shape and without changing its frequency is known as amplification.

A device which increases the amplitude of the input signal is called amplifier.

A transistor can be used as an amplifier in active state.

A basic circuit of a common emitter transistor amplifier is shown.



LOGIC GATES

INTRODUCTION :

- A logic gate is a digital circuit which is based on certain logical relationship between the input and the output voltages of the circuit.
- The logic gates are built using the semiconductor diodes and transistors.
- Each logic gate is represented by its characteristic symbol.
- The operation of a logic gate is indicated in a table, known as truth table. This table contains all possible combinations of inputs and the corresponding outputs.
- A logic gate is also represented by a Boolean algebraic expression. Boolean algebra is a method of writing logical equations showing how an output depends upon the combination of inputs. Boolean algebra was invented by George Boole.

BASIC LOGIC GATES

There are three basic logic gates. They are (1) OR gate (2) AND gate, and (3) NOT gate

- **The OR gate :-** The output of an OR gate attains the state 1 if one or more inputs attain the state 1.

Logic symbol of OR gate

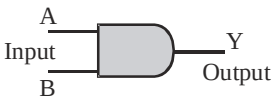
The Boolean expression of OR gate is Y = A + B, read as Y equals A 'OR' B.

Truth table of a two-input OR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

- **The AND gate :-** The output of an AND gate attains the state 1 if and only if all the inputs are in state 1.

Logic symbol of AND gate



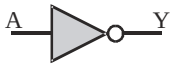
The Boolean expression of AND gate is Y = A.B

It is read as Y equals A 'AND' B

Truth table of a two-input AND gate

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

- **The NOT gate :** The output of a NOT gate attains the state 1 if and only if the input does not attain the state 1.

  Logic symbol of NOT gate 

  The Boolean expression is $Y = \overline{A}$, read as Y equals NOT A.

  Truth table of NOT gate

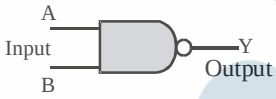
A	Y
0	1
1	0

COMBINATION OF GATES :

The three basis gates (OR, AND and NOT) when connected in various combinations give us logic gates such as NAND, NOR gates, which are the universal building blocks of digital circuits.

- **The NAND gate :**

  Logic symbol of NAND gate



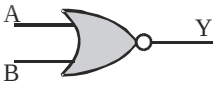
  The Boolean expression of NAND gate is $Y = \overline{A.B}$

  Truth table of a NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

- **The NOR gate :**

  Logic symbol of NOR gate



  The Boolean expression of NOR gate is $Y = \overline{A + B}$

  Truth table of a NOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

UNIVERSAL GATES :

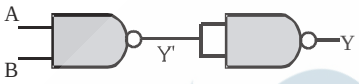
The NAND or NOR gate is the universal building block of all digital circuits. Repeated use of NAND gates (or NOR gates) gives other gates. Therefore, any digital system can be achieved entirely from NAND or NOR gates. We shall show how the repeated use of NAND (and NOR) gates will gives us different gates.

- **The NOT gate from a NAND gate :-** When all the inputs of a NAND gate are connected together, as shown in the figure, we obtain a NOT gate

Truth table of a single input NAND gate

A	B= (A)	Y
0	0	1
1	1	0

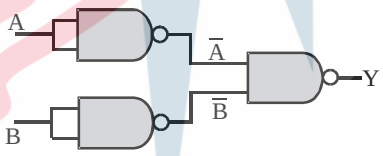
- **The AND gate from a NAND gates :-** If a NAND gate is followed by a NOT gate (i.e., a single input NAND gate), the resulting circuit is an AND gate as shown in figure and truth table given show how an AND gate has been obtained from NAND gates.



Truth table

A	B	Y'	Y
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

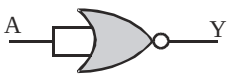
- **The OR gate from NAND gates :-** If we invert the inputs A and B and then apply them to the NAND gate, the resulting circuit is an OR gate.



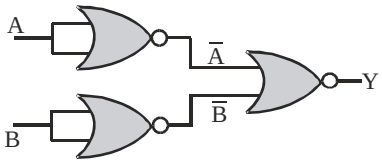
Truth table

A	B	$\overline{A}$	$\overline{B}$	Y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

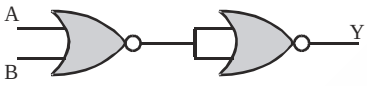
- **The NOT gate from NOR gates :-** When all the inputs of a NOR gate are connected together as shown in the figure, we obtain a NOT gate



- The AND gate from NOR gates :- If we invert the inputs A and B and then apply them to the NOR gate, the resulting circuit is an AND gate.



- **The OR gate from NOR gate :-** If a NOR gate is followed by a single input NOR gate (NOT gate), the resulting circuit is an OR gate.



XOR AND XNOR GATES :

- **The Exclusive - OR gate (XOR gate):-** The output of a two-input XOR gate attains the state 1 if one and only one input attains the state 1.

  Logic symbol of XOR gate

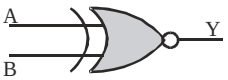
  The Boolean expression of XOR gate is $Y = A.\overline{B} + \overline{A}.B$ or $Y = A \oplus B$

  Truth table of a XOR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

- **Exclusive - NOR gate (XNOR gate):-** The output is in state 1 when its both inputs are the same that is, both 0 or both 1.

  Logic symbol of XNOR gate

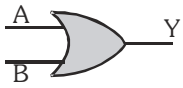
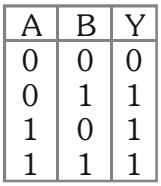
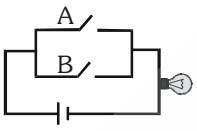
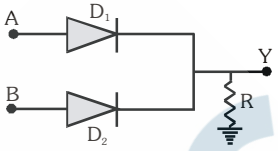
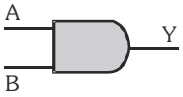
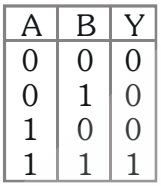
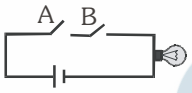
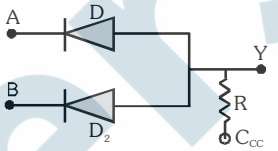
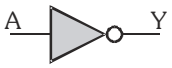
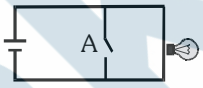
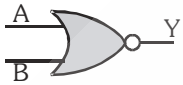
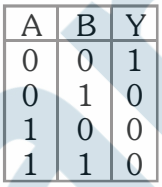
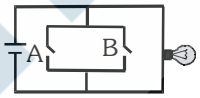
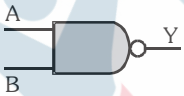
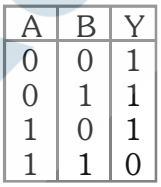
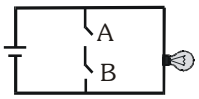
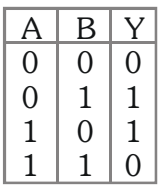
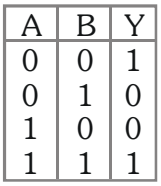


  The Boolean expression of XNOR gate is $Y = A.B + \overline{A}.\overline{B}$ or $Y = \overline{A \oplus B}$ or $A \odot B$

  Truth table of a XNOR gate

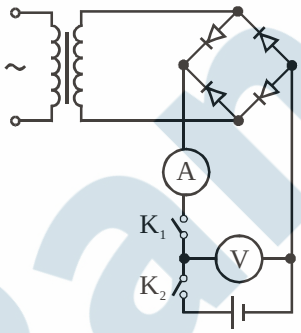
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

SUMMARY OF LOGIC GATES

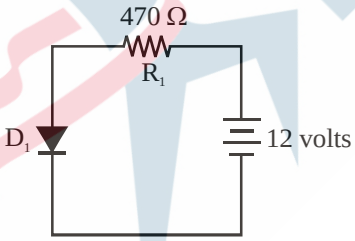
Names	Symbol	Boolean Expression	Truth table	Electrical analogue	Circuit diagram (Practical Realisation)
OR		$Y = A + B$			
AND		$Y = A.B$			
NOT Inverter		$Y = \overline{A}$			
NOR (OR +NOT)		$Y = \overline{A + B}$			
NAND (AND+NOT)		$Y = \overline{A.B}$			
XOR (Exclusive OR)		$Y = A \oplus B$ or $Y = \overline{A}.B + A\overline{B}$			
XNOR (Exclusive NOR)		$Y = A \odot B$ or $Y = A.B + \overline{A}.\overline{B}$ or $Y = \overline{A \oplus B}$			

EXERCISE-S

1. The battery is charged from full wave rectifier fed by a sinusoidal voltage (see figure). Ideal diodes, ammeter and voltmeter show the time-average value. At idle with only key K_1 closed, voltmeter shows 12 V, and current is then absent, ie, reading of ammeter is 0. If only the key K_2 is closed, the voltmeter shows battery voltage at 12.3 V. During charging, when the K_2 and K_1 are closed, the voltmeter shows 12.8 V and ammeter shows 5 A. Find the internal resistance of battery.

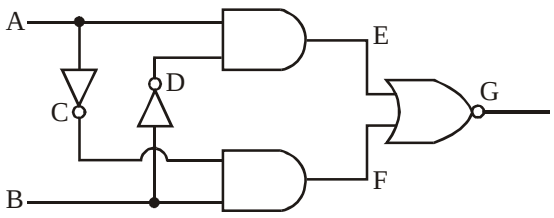


2. Complete the following table of values for this diode circuit, assuming a typical forward voltage drop of 0.65 volts for the diode:

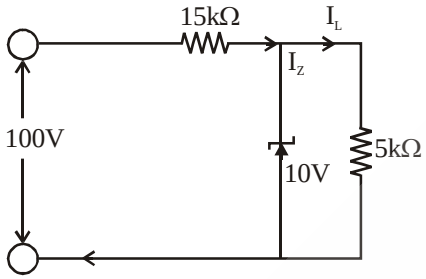


	R_1	D_1	Total
V			12 V
I			
R	470 Ω		
P			

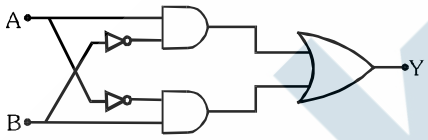
3. Write a truth table for the circuit in figure, including the states at C, D, E, F and G.



4. For the circuit shown in figure, find
i) the output voltage
ii) the voltage drop across series resistance
iii) the current through zener diode.



5. Write down the actual logic operation carried by the following circuit. Explain your answer.



EXERCISE-O

SINGLE CORRECT TYPE QUESTIONS

1. An electric field is applied to a semi-conductor. Let the number of charge carriers be n and the average drift speed be v. If the temperature is increased

(A) Both n and v will increase (B) n will increase but v will decrease

(C) v will increase but n will decrease (D) Both n and v will decrease

2. The manifestation of band structure in solids is due to - **[AIEEE-2004]**

(A) Bohr's correspondence principle (B) Pauli's exclusion principle

(C) Heisenberg's uncertainty principle (D) Boltzmann's law

3. P-type semiconductor is formed when

A. As impurity is mixed in Si B. Al impurity is mixed in Si

C. B impurity is mixed in Ge D. P impurity is mixed in Ge

(A) A and C (B) A and D (C) B and C (D) B and D

4. In extrinsic semiconductors -

(A) The conduction band and valence band overlap

(B) The gap between conduction band and valence band is more than 16 eV

(C) The gap between conduction band and valence band is near about 1 eV

(D) The gap between conduction band and valence band will be 100 eV and more

5. A strip of copper and another of germanium are cooled from room temperature to 80 K. The resistance of - **[AIEEE-2004]**

(A) copper strip increases and that of germanium decreases

(B) copper strip decreases and that of germanium increases

(C) each of these increases

(D) each of these decreases

6. In a P-N junction diode not connected to any circuit -

(A) the potential in the same everywhere

(B) the P-type side is at a higher potential then the N-type side

(C) there is an electric field at the junction directed from the N-type side to the P-type side

(D) there is an electric field at the junction directed from the P-type to the N-type side

7. When p-n junction diode is forward biased, then. **[AIEEE-2004]**

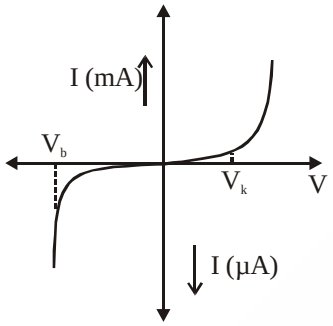
(A) both the depletion region and barrier height are reduced

(B) the depletion region is widened and barrier height is reduced

(C) the depletion region is reduced and barrier height is increased

(D) both the depletion region and barrier height are increased

8. The V-I characteristic for a p-n junction diode is plotted as shown in the figure. From the plot we can conclude that [$V_b \rightarrow$ breakdown voltage, $V_k \rightarrow$ knee voltage]



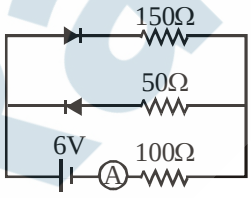
(A) the forward bias resistance of diode is very high; almost infinity for small values of V and after a certain value it becomes very low

(B) the reverse bias resistance of diode is very high in the beginning upto breakdown voltage is not achieved

(C) both forward and reverse bias resistances are same for all voltages

(D) both (A) and (B) are correct

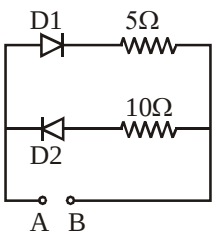
9. In the below given arrangement determine the ammeter reading, if each diodes have a forward resistance of 50 Ω and infinite backward resistance -



(A) zero (B) 0.02 (C) 0.03 (D) 0.036

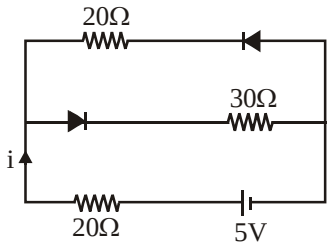
10. A 2V battery is connected across AB as shown in the figure. The value of the current supplied by the battery when in one case battery's positive terminal is connected to A and in other case when positive terminal of battery is connected to B will respectively be :-

(JEE-Main Online-2015)



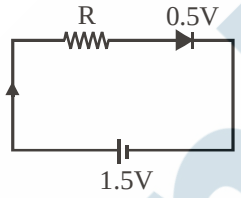
(A) 0.1 A and 0.2 A (B) 0.4 A and 0.2 A (C) 0.2 A and 0.4 A (D) 0.2 A and 0.1 A

11. Current in the circuit will be -



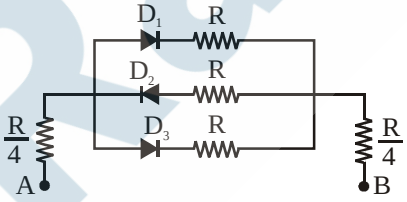
(A) $\frac{5}{40}$A (B) $\frac{1}{10}$A (C) $\frac{5}{10}$A (D) $\frac{5}{20}$A

12. The diode used in the circuit shown in the figure has a constant voltage drop of 0.5 V at all currents and a maximum power rating of 100 milliwatts. What should be the value of the resistor R connected in series with the diode for obtaining maximum current -



(A) 1.5 Ω (B) 5 Ω (C) 6.67 Ω (D) 200 Ω

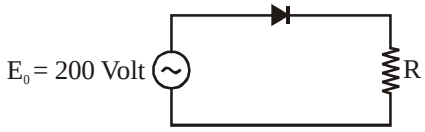
13. In the following circuits PN-junction diodes D_1, D_2 and D_3 are ideal for the following potential of A and B, the correct increasing order of resistance between A and B will be -



(i) –10V, –5V, (ii) –5V, –10V (iii) –4V, –12V

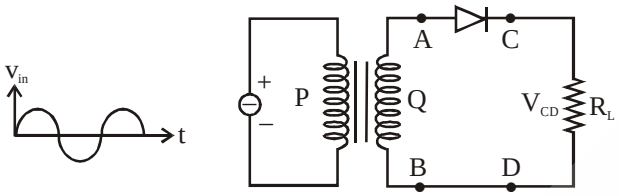
(A) (i) < (ii) < (iii) (B) (iii) < (ii) < (i) (C) (ii) = (iii) < (i) (D) (i) = (iii) < (ii)

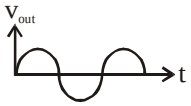
14. A sinusoidal voltage of peak value 200 volt is connected to a diode and resistor R in the circuit shown so that half wave rectification occurs. If the forward resistance of the diode is negligible compared to R then rms voltage (in volt) across R is approximately -



(A) 200 (B) 100 (C) $\frac{200}{\sqrt{2}}$ (D) 280

15. In the half-wave rectifier circuit shown. Which one of the following wave forms is true for V_{CD}, if the input is as shown?



(A) 

(B) 

(C) 

(D) 

16. Zener diode is a p-n junction which has -

(A) p-end heavily doped, n-end lightly doped

(B) n-end heavily doped, p-end lightly doped

(C) both p and n-ends heavily doped

(D) both p and n-ends lightly doped

17. Zener diode has both p and n-ends heavily doped so that -

(A) it has small thickness of depletion region

(B) it has large thickness of depletion region due to large recombination

(C) it has large reverse bias voltage

(D) it has weak reverse current when reverse biased

18. Most important use of zener diode is to have –

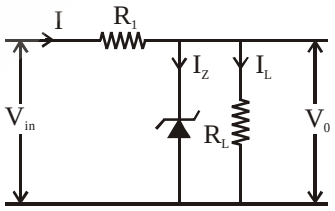
(A) constant voltage across applied load

(B) any desired current at constant voltage

(C) a p-n junction working under constant regulated voltage conditions

(D) a p-n junction to operate at high voltages

19. In given figure when input voltage increases,



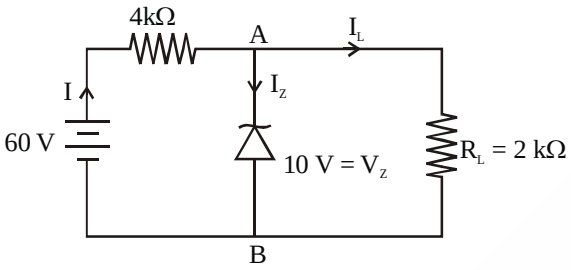
(A) the current through R_S, R_L and zener increases

(B) the current through R_S increases, zener increases but through R_L remains constant

(C) the current through R_S increases, through zener decreases, R_L increases

(D) the current through R_S increases, through zener remains constant but R_L increases

20. A Zener diode is connected to a battery and a load as shown below. The currents I, I_Z and I_L are respectively. **(JEE-Main Online-2014)**



(A) 12.5 mA, 5 mA, 7.5 mA (B) 15 mA, 7.5 mA, 7.5 mA
(C) 12.5 mA, 7.5 mA, 5 mA (D) 15 mA, 5 mA, 10 mA

21. A transistor is used in common emitter mode as an amplifier, then:
(1) the base emitter junction is forward biased
(2) the base emitter junction is reverse biased
(3) the input signal is connected in series with the voltage applied to bias the base emitter junction
(4) the Input signal is connected is series with the voltage applied to bias the base collector junction which is correct-
(A) 1, 2, 3 (B) 1, 2, 3, 4 (C) 1, 3 (D) 2, 3, 4

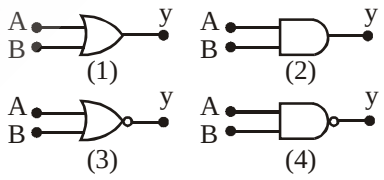
22. In a n-p-n transistor circuit the collector current is 10 mA. If 90% of the electron emitted reach the collector then -
(A) the emitter current will be 9 mA (B) the base current will be 9 mA
(C) the emitter current will be 11 mA (D) the base current will be -1 mA

23. n-p-n transistors are preferred to p-n-p transistors because -
(A) they have low cost (B) they have low dissipation energy
(C) they are capable of handling large power (D) electrons have high mobility than holes.

24. When npn transistor is used as an amplifier **[AIEEE-2004]**
(A) electrons move from collector to base (B) holes move from emitter to base .
(C) electrons move from base to collector (D) holes move from base to emitter

25. For a transistor, α is 0.8. The transistor is in CE configuration. The change in the collector current when the base current changes by 6 mA is :-
(A) 6 mA (B) 4.8mA (C) 24mA (D) 8mA

26. Given below are four logic gate symbol (figure). Those for OR, NOR and NAND are respectively



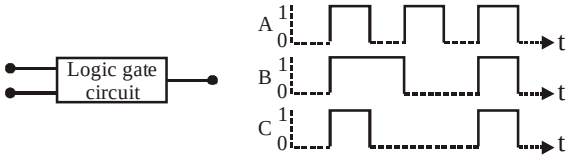
(A) 1,4,3 (B) 4,l,2 (C) l,3,4 (D) 4,2,l

27. The following truth table corresponds to the logic gate -

A	0	0	1	1
B	0	1	0	1
X	0	1	1	1

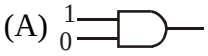
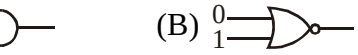
(A) NAND (B) OR (C) AND (D) XOR

28. The following figure shows a logic gate circuit with two input A and B output C. The voltage waveforms of A, B and C are as shown in second figure below. The logic gate is :



(A) OR gate (C) NAND gate (B) AND gate (D) NOR gate

29. Which of the following gates will have an output of 1 -

(A)  (B)  (C)  (D) 

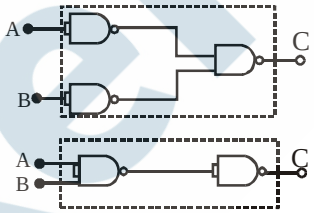
30. The combination of 'NAND' gates shown here under (figure) are equivalent to -

(A) An OR gate and an AND gate respectively

(B) An AND gate and a NOT gate respectively

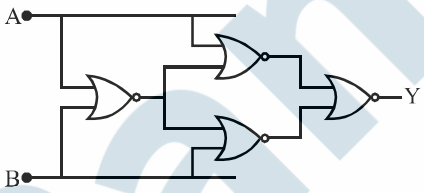
(C) An AND gate and an OR gate respectively

(D) An OR gate and a NOT gate respectively



31. A system of four gates is set up as shown.The 'truth table' corresponding to this system is :-

(JEE-Main Online-2013)



(A)

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

(B)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

(C)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

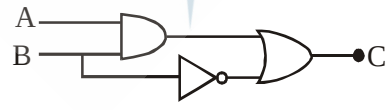
(D)

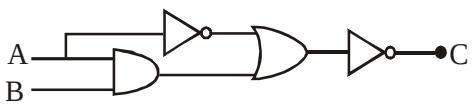
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

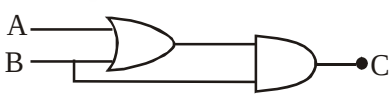
32. Which of the following circuits correctly represents the following truth table ?

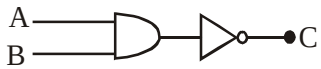
(JEE-Main Online-2013)

A	B	C
0	0	0
0	1	0
1	0	1
1	1	0

(A) 

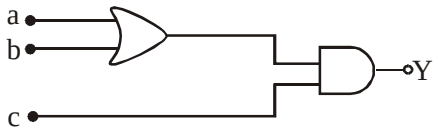
(B) 

(C) 

(D) 

33. To get an output of 1 from the circuit shown in figure the input must be :-

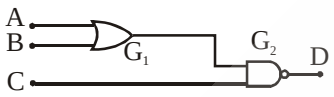
(JEE-Main Online-2016)



(A) a = 1, b = 0, c = 1 (B) a = 1, b = 0, c = 0

(C) a = 0, b = 1, c = 0 (D) a = 0, b = 0, c = 1

34. For the given combination of gates, if the logic states of inputs A, B, C are as follows A = B = C = 0 and A = B = 1, C = 0 then the logic states of output D are -

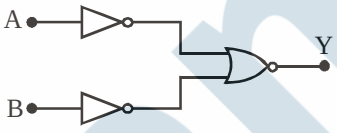


(A) 0, 0 (B) 0, 1 (C) 1, 0 (D) 1,1

35. This symbol represents

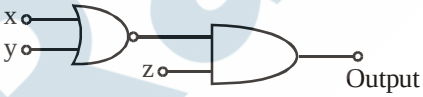
(A) NOT gate (B) OR (C) AND gate (D) NOR gate

36. Which logic gate is represented by the following combination of logic gates -



(A) OR (B) NAND (C) AND (D) NOR

37. In which of the following cases, we would obtain an output of one.



(A) x = l, y = l, z = l (B) x = l, y = l, z = 0 (C) x = 0, y = l, z = l (D) x = 0, y = 0, z = l

38. In a full wave rectifier circuit operating from 50 Hz mains frequency, the fundamental frequency in the ripple would be :- **[AIEEE-2005]**

(A) 50 Hz (B) 25Hz (C) 100 Hz (D) 70.7 Hz

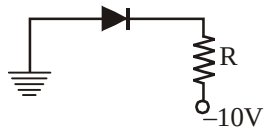
39. The electrical conductivity of a semiconductor increases when electromagnetic radiation of wavelength shorter than 2480 nm is incident on it. The band gap (in eV) for the semiconductor is **[AIEEE-2005]**

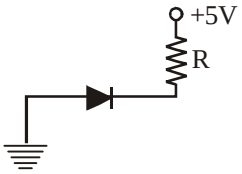
(A) 1.1 eV (B) 2.5 eV (C) 0.5 eV (D) 0.7 eV

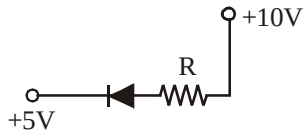
40. If the ratio of the concentration of electrons to that of holes in a semiconductor is $\frac{7}{5}$ and the ratio of currents is $\frac{7}{4}$ then what is the ratio of their drift velocities - **[AIEEE-2006]**

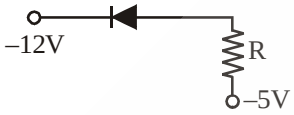
(A) $\frac{5}{4}$ (B) $\frac{4}{7}$ (C) $\frac{5}{6}$ (D) $\frac{4}{5}$

41. In the following, which one of the diodes is reverse biased ; **[AIEEE-2006]**

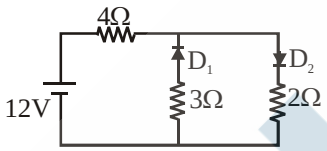
(A) 

(B) 

(C) 

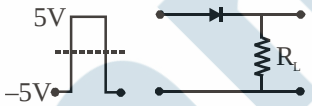
(D) 

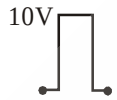
42. The circuit has two oppositely connected ideal diodes in parallel. What is the current flowing in the circuit ? **[AIEEE-2006]**

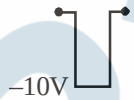


(A) 2.31 A (B) 1.33 A (C) 1.71 A (D) 2.00 A

43. If in a p-n junction diode, a square input signal of 10V is applied as shown. Then the output signal across R_L will be :- **[AIEEE-2007]**



(A) 

(B) 

(C) 

(D) 

44. Carbon, silicon and germanium have four valence electrons each. At room temperature which one of the following statements is most appropriate ? **[AIEEE-2007]**

(A) The number of free conduction electrons is significant in C but small in Si and Ge

(B) The number of free conduction electrons is negligibly small in all the three

(C) The number of free electrons for conduction is significant in all the three

(D) The number of free electrons for conduction is significant only in Si and Ge but small in C

MULTIPLE CORRECT TYPE QUESTIONS

45. Which of the following statements is correct

(A) Resistance of semiconductor decreases with increase in temperature

(B) In an electric field, displacement of holes is opposite to the displacement of electrons

(C) Resistance of a conductor decreases with the increase in temperature

(D) n-type semiconductors are neutral

46. Pick out the correct statement the reverse current in p-n junction diode

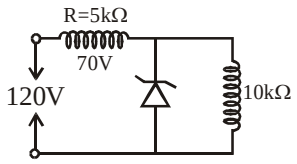
(A) can be minimum and constant

(B) remains constant even after the breakdown voltage

(C) becomes infinity at breakdown

(D) reverse current is controlled by external resistance

47. For the circuit shown in the figure:



(A) current through zener diode is 4 mA (B) current through zener diode is 9 mA

(C) the output voltage is 50 V (D) the output voltage is 40 V

48. Which of the following devices are heavily doped p-n junction

(A) Photo diode (B) Light emitting diode

(C) Solar cell (D) Zener mode

49. Which of the following statements is correct for proper working of zener diode ?

(A) Reverse bias voltage should be less than or equal to zener breakdown voltage

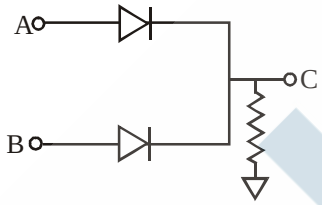
(B) Reverse bias voltage applied must be greater than zener breakdown voltage.

(C) Zener is to be reverse biased for zener action

(D) For given zener diode there can be different zener breakdown voltages

EXERCISE-JM

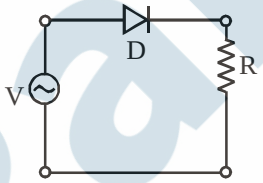
1. In the circuit below, A and B represent two inputs and C represents the output. **[AIEEE-2008]**



The circuit represents

(1) AND gate (2) NAND gate (3) OR gate (4) NOR gate

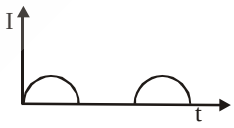
2. An p-n junction (D) shown in the figure can act as a rectifier. An alternating current source (V) is connected in the circuit.

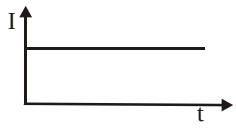


The current (I) in the resistor R can be shown by: **[AIEEE-2009]**

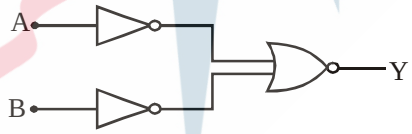
(1) 

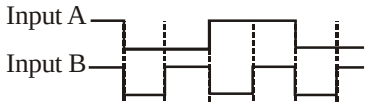
(2) 

(3) 

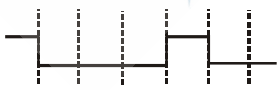
(4) 

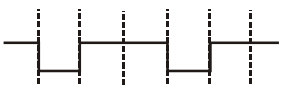
3. The logic circuit shown below has the input wave forms 'A' and 'B' as shown. Pick out the correct output waveform. **[AIEEE-2009]**





Output is -

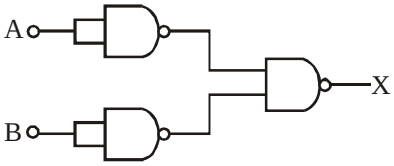
(1) 

(2) 

(3) 

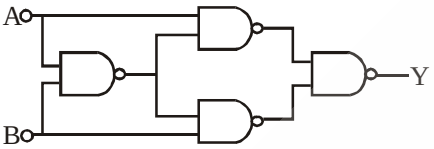
(4) 

4. The combination of gates shown below yields. **[AIEEE-2010]**



(1) XOR gate (2) NAND gate (3) OR gate (4) NOT gate

5. Truth table for system of four NAND gates as shown in figure is: **[AIEEE-2012]**



(1)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

(2)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

(3)

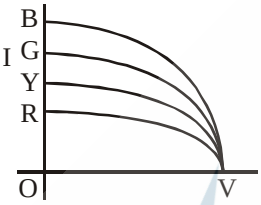
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(4)

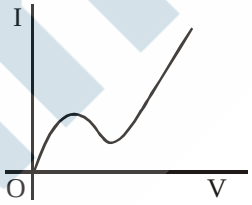
A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

6. The I-V characteristic of an LED is **[JEE Main 2013]**

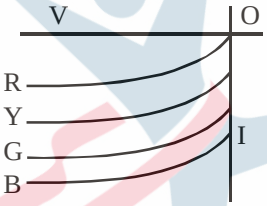
(1)



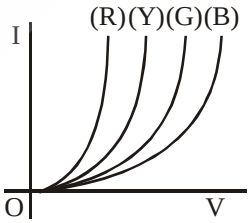
(2)



(3)

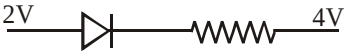


(4)

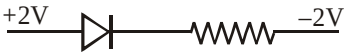


7. The forward biased diode connection is: **[JEE Main-2014]**

(1) 

(2) 

(3) 

(4) 

8. For a common emitter configuration, if α and β have their usual meanings, the **incorrect** relationship between α and β is **[JEE Main-2016]**

(1) $\alpha = \frac{\beta^2}{1+\beta^2}$ (2) $\frac{1}{\alpha} = \frac{1}{\beta} + 1$ (3) $\alpha = \frac{\beta}{1-\beta}$ (4) $\alpha = \frac{\beta}{1+\beta}$

9. If a, b, c, d are inputs to a gate and x is its output, then as per the following time graph, the gate is **[JEE Main-2016]**

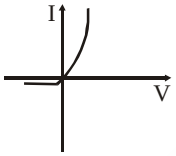
(d)
(c)
(b)
(a)
(x)

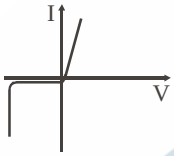
(1) NAND (2) NOT (3) AND (4) OR

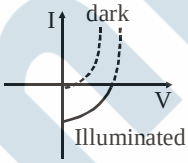
10. The temperature dependence of resistances of Cu and undoped Si in the temperature range 300-400K, is best described by :- **[JEE Main-2016]**

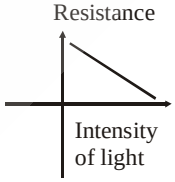
(1) Linear decrease for Cu, linear decrease for Si.
(2) Linear increase for Cu, linear increase for Si.
(3) Linear increase for Cu, exponential increase for Si
(4) Linear increase for Cu, exponential decrease for Si

11. Identify the semiconductor devices whose characteristics are given below, in the order (a), (b), (c), (d):- **[JEE Main-2016]**

(a) 

(b) 

(c) 

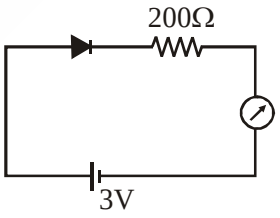
(d) 

(1) Zener diode, Solar cell, Simple diode, Light dependent resistance
(2) Simple diode, Zener diode, Solar cell, Light dependent resistance
(3) Zener diode, Simple diode, Light dependent resistance, Solar cell
(4) Solar cell, Light dependent resistance, Zener diode, Simple diode

12. In a common emitter amplifier circuit using an n-p-n transistor, the phase difference between the input and the output voltages will be : **[JEE Main-2017]**

(1) 135° (2) 180° (3) 45° (4) 90°

13. The reading of the ammeter for a silicon diode in the given circuit is :- **[JEE Main-2018]**



(1) 15 mA (2) 11.5 mA (3) 13.5 mA (4) 0

CBSE Previous Year's Questions

1. Draw the voltage current characteristic of a zener diode. **[1; CBSE-2004]**

2. With the help of a labelled circuit diagram, explain how an n-p-n transistor can be used as an amplifier in common-emitter configuration. Explain how the input and output voltages are out of phase by 180° for a common-emitter transistor amplifier. **[5; CBSE-2004]**

3. How does the resistivity of (i) a conductor and (ii) a semiconductor vary with temperature? Give reason for each case. **[2; CBSE-2005]**

4. On the basis of the energy band diagrams. Distinguish between metals, insulators and semiconductors. **[3; CBSE-2005]**

5. (a) With the help of a circuit diagram explain the working of transistor as oscillator.

(b) Draw a circuit diagram for a two input OR gate and explain its working with the help of input, output waveforms. **[5; CBSE-2005]**

6. (a) Explain briefly with the help of a circuit diagram, how V -1 characteristics of a p-n junction diode are obtained in (i) forward bias, and (ii) reverse bias.

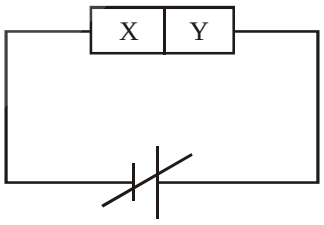
(b) A photodiode is fabricated from a semiconductor with a band gap of 2.8 eV. Can it detect wave length of 6000 nm? Justify. **[5; CBSE-2005]**

7. Explain (i) forward biasing, (ii) reverse biasing of a P-N junction diode. With the help of a circuit diagram, explain the use of this device as a half - wave rectifier. **[3; CBSE-2006]**

8. What are energy bands? How are these formed? Distinguish between a conductor, an insulator and a semiconductor on the basis of energy band diagram. **[5; CBSE-2006]**

9. Explain the function of base region of a transistor. Why is this region made thin and lightly doped? Draw a circuit diagram to study the input and output characteristics of n-p-n transistor in a common emitter (CE) configuration. Show these characteristics graphically. Explain how current amplification factor of the transistor is calculated using output characteristics. **[5; CBSE-2006]**

10. Two semiconductor materials X and Y shown in the given figure, are made by doping germanium crystal with indum and arsenic respectively. The two are joined end to end and connected to a battery as shown. **[2; CBSE-2007]**



(i) Will the junction be forward biased or reverse biased ?

(ii) Sketch a V-I graph for this arrangement.

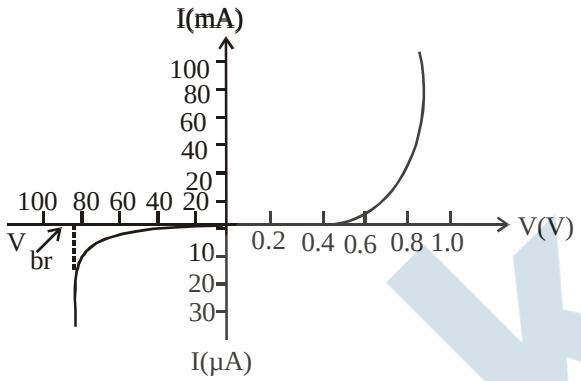
11. Draw the circuit diagram of a common emitter amplifier using n-p-n transistor. What is the phase difference between the input signal and output voltage ? State two reasons why a common emitter amplifier is preferred to a common base amplifier. **[3; CBSE-2007]**

12. Explain the formation of energy band in solids. Draw energy band diagram for (i) a conductor, (ii) an intrinsic semiconductor. **[3; CBSE-2007]**

13. Write the acronym LASER in expanded form. State any four reasons for preferring diode lasers as light sources for optical communication links. **[3; CBSE-2007]**

14. Distinguish between an intrinsic semiconductor and P-type semiconductor. Give reason, why, a P-type semiconductor crystal is electrically neutral, although $n_h >> n_e$? **[2; CBSE-2008]**

15. The figure below shows the V-I characteristic of a semiconductor diode.

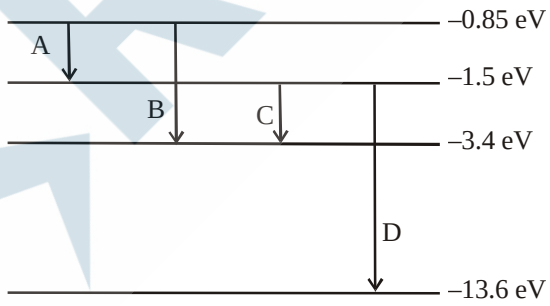


(i) Identify the semiconductor diode used.

(ii) Draw the circuit diagram to obtain the given characteristic of this device.

(iii) Briefly explain how this diode can be used as a voltage regulator. **[3; CBSE-2008]**

16. The energy level diagram of an element is given below. Identify, by doing necessary calculations, which transition corresponds to emission of a spectral line of wavelength 102.7 nm.



[3; CBSE-2008]

17. (i) Draw a circuit diagram to study the input and output characteristics of an n-p-n transistor in its common emitter configuration. Draw the typical input and output characteristics.

(ii) Explain, with the help of a circuit diagram, the working of n -p-n transistor as a common emitter amplifier. **[5; CBSE-2009]**

18. How is a zener diode fabricated so as to make it a special purpose diode? Draw I -V characteristics of zener diode and explain the significance of break down voltage. Explain briefly, with the help of a circuit diagram, how a-p-n junction diode work **[5; CBSE-2009]**

19. (a) Draw the circuit diagram of a p-n junction diode in (i) forward bias, (ii) reverse bias. How are these circuits used to study the V-I characteristics of a silicon diode ? Draw the typical V-I characteristics.

(b) What is a light emitting diode (LED)? Mention two important advantages of LEDs over conventional lamps. **[5; CBSE-2010]**

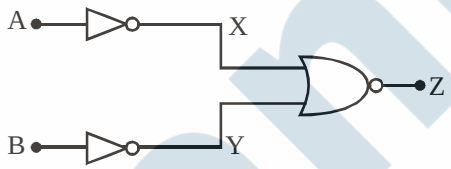
20. (a) Draw the circuit arrangement for studying the input and output characteristics of an n-p-n transistor in CE configuration. With the help of these characteristics define (i) input resistance, (ii) current amplification factor.

(b) Describe briefly with the help of a circuit diagram how an n-p-n transistor is used to produce self-sustained oscillations. **[5; CBSE-2010]**

21. What happens to the width of depletion layer of a p-n junction when it is (i) forward biased, (ii) reverse biased? **[1; CBSE-2011]**

22. Draw a labelled diagram of a full wave rectifier circuit. State its working principle. Show the input-output waveforms. **[3; CBSE-2011]**

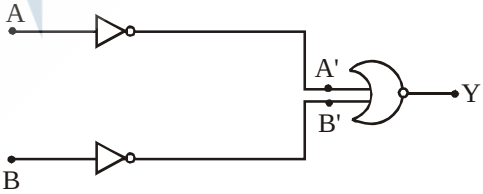
23. You are given a circuit below. Write its truth table, hence, identify the logic operation carried out by this circuit. Draw the logic symbol of the gate it corresponds to. **[3; CBSE-2011]**



24. Describe briefly with the help of a circuit diagram, how the flow of current carries in a p-n-p transistor is regulated with emitter-base junction forward and base-collector junction reverse biased. **[2;CBSE-2012]**

25. (a) Describe briefly, with the help of a diagram, the role of the two important processes involved in the formation of a p-n junction

(b) Name the device which is used as a voltage regulator. Draw the necessary circuit diagram and explain its working



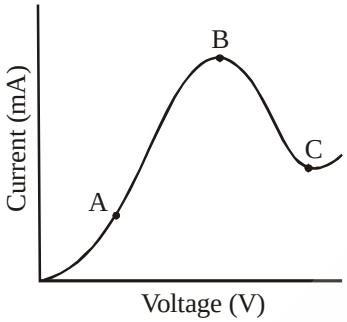
OR

(a) Explain briefly the principle on which a transistor-amplifier works as an oscillator. Draw the necessary circuit diagram and explain its working.

(b) Identify the equivalent gate for the following circuit and write its truth table. **[5; CBSE-2012]**

26. The graph shown in the figure represents a plot of current versus voltage for a given semiconductor. Identity the region, if any, over which the semiconductor has a negative resistance.

[3; CBSE-2013]



27. Draw typical output characteristics of an n-p-n transistor in CE configuration. Show how these characteristics can be used to determine output resistance. **[5; CBSE-2013]**

OR

28. Draw V -1 characteristics of a-p-n junction diode. Answer the following questions, giving reasons:
(i) Why is the current under reverse bias almost independent of the applied potential upto a critical voltage?
(ii) Why does the reverse current show a sudden increase at the critical voltage ?
Name any semiconductor device which operates under the reverse bias in the breakdown region.
[5; CBSE-2013]

29. Draw a circuit diagram of n-p-n transistor amplifier in CE configuration. Under what condition does the transistor acts as an amplifier ? **[2; CBSE-2014]**

30. Explain, with the help of a circuit diagram, the working of a p-n junction diode as a half-wave rectifier. **[2; CBSE-2014]**

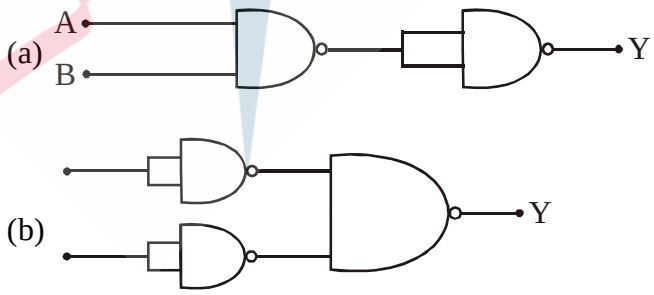
31. Write any two distinguishing features between conductors, semiconductors and insulators on the basis of energy band diagrams. **[3; CBSE-2014]**

32. With the help of a circuit diagram, explain the working of a junction diode as a full wave rectifier. Draw its input and output waveforms. Which characteristic property makes the junction diode suitable for rectification ? **[3; CBSE-2015]**

33. The outputs of two NOT gates are fed to a NOR gate. Draw the logic circuit of the combination of gates. Write its truth table. Identify the gate equivalent to this circuit. **[3; CBSE-2015]**

OR

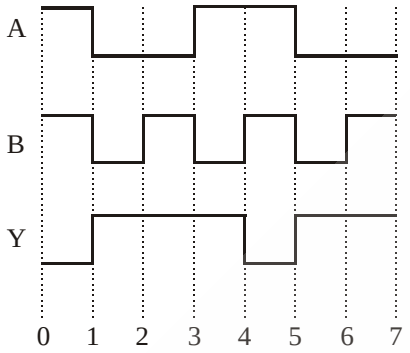
You are given two circuits (a) and (b) as shown in the figures, which consist of NAND gates. Identify the ligic operation carried out by the two. Write the truth tables for each. Identify the gates equivalent to the two circuits.



[3; CBSE-2015]

34. (i) Name two important processes that occur during the formation of a pn junction.
(ii) Draw the circuit diagram of a full wave rectifier along with the inpur and output waveforms. Briefly explain how the output voltage/current is unidirectional. **[CBSE-2016]**

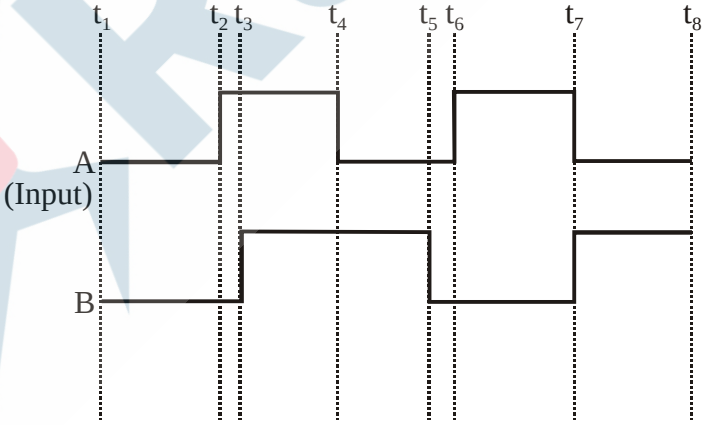
35. (i) Distinguish between a conductor and a semi conductor on the basis of energy band diagram.
(ii) The following figure shows the input waveforms (A, B) and the output waveform (Y) of a gate. Identify the gate, write its truth table and draw its logic symbol. **[CBSE-2016]**



36. (a) In the following diagram, is the junction diode forward biased or reverse biased ? **[CBSE-2017]**

(b) Draw the circuit diagram of a full wave rectifier and state how it works.

37. (a) Write the functions of the three segments of a transistor. **[CBSE-2017]**
(b) The figure shows the input waveforms A and B for 'AND' gate. Draw the output waveform and write the truth table for this logic gate.



38. (a) A student wants to use two p-n junction diodes to convert alternating current into direct current. Draw the labelled circuit diagram she would use and explain how it works.
(b) Give the truth table and circuit symbol for NAND gate. **[CBSE-2018]**

39. Draw the typical input and output characteristics of an n-p-n transistor in CE configuration. Show how these characteristics can be used to determine (a) the input resistance (r_i) and (b) current amplification factor (β). **[CBSE-2018]**

ANSWER KEY

EXERCISE-S

1. Ans. 0.1 Ω

2. Ans.

	R_1	D_1	Total
V	11.35V	0.65V	12V
I	24.15 mA	24.15 mA	24.15 mA
R	470 Ω		
P	274.1 mW	15.7 mW	289.8 mW

3. Ans.

A	B	C	D	E	F	G
0	0	1	1	0	0	1
0	1	1	0	0	1	0
1	0	0	1	1	0	0
1	1	0	0	0	0	1

4. Ans. (i) 10 V (ii) 90 V (iii) 4 mA

EXERCISE-O

SINGLE CORRECT TYPE QUESTIONS

1. Ans. (B) **2. Ans. (B)** **3. Ans. (C)** **4. Ans. (C)** **5. Ans. (B)** **6. Ans. (C)**
7. Ans. (A) **8. Ans. (D)** **9. Ans. (B)** **10. Ans. (B)** **11. Ans. (B)** **12. Ans. (B)**
13. Ans. (C) **14. Ans. (B)** **15. Ans. (B)** **16. Ans. (C)** **17. Ans. (A)** **18. Ans. (A)**
19. Ans. (B) **20. Ans. (C)** **21. Ans. (C)** **22. Ans. (C)** **23. Ans. (D)** **24. Ans. (C)**
25. Ans. (C) **26. Ans. (C)** **27. Ans. (B)** **28. Ans. (C)** **29. Ans. (C)** **30. Ans. (A)**
31. Ans. (D) **32. Ans. (B)** **33. Ans. (A)** **34. Ans. (D)** **35. Ans. (A)** **36. Ans. (C)**
37. Ans. (D) **38. Ans. (C)** **39. Ans. (C)** **40. Ans. (A)** **41. Ans. (B)** **42. Ans. (D)**
43. Ans. (D) **44. Ans. (D)**

MULTIPLE CORRECT TYPE QUESTIONS

45. Ans. (A,B,D) **46. Ans. (A,C,D)** **47. Ans. (B,C)** **48. Ans. (B,D)** **49. Ans. (B,C)**

EXERCISE-JM

1. Ans. (3) **2. Ans. (3)** **3. Ans. (1)** **4. Ans. (3)** **5. Ans. (3)** **6. Ans. (4)**
7. Ans. (4) **8. Ans. (1 or 3)** **9. Ans. (4)** **10. Ans. (4)** **11. Ans. (2)** **12. Ans. (2)**
13. Ans. (2)